A Stability-Informed Design Approach for RF Circuits

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***Abstract*—This work presents a stability-informed design approach for microwave circuits, which uses multiple complementary metrics that provide designers with information required to ensure circuit stability. Bilateral loop gain (BLG) and driving point immittance (DPI) are employed to analyze feedback loops and nodal impedances, enabling designers to monitor and resolve stability issues throughout the design process. The approach is presented and its use demonstrated in the design of a 20–40 GHz SiGe amplifier, using both simulation and measurement results.**

***Index Terms*—SiGe BiCMOS, microwave amplifier, stability analysis, bilateral loop gain, driving point immittance**

I. Introduction

High-performance microwave circuits require stability analysis and design techniques to prevent unwanted oscillations. Circuits with multiple stages and active devices are particularly susceptible to spurious oscillations, due to the presence of many feedback loops. This has led to the creation of different stability metrics to help designers ensure stability in their circuits.

One commonly used metric is Rollet's K-factor, which allows for quick evaluation and can provide useful information, but is a global metric and can miss instabilities in internal nodes of multistage circuits [1]. Methods such as the Mu-factor and the Nyquist test provide more information, but fail to show certain instabilities. Finally, the Normalized Determinant Function (NDF) and Ohtomo's Network Bifurcation [2] have been demonstrated as rigorous methods, but are often impractical to implement.

The present paper proposes a practical design approach leveraging both bilateral loop gain and driving point immittance. The approach enables identification of problematic nodes and loops in a given circuit, and provides information about the specific oscillation frequencies during the design process. The designer can then use this information to quickly stabilize the circuit. Finally, a 20–40 GHz SiGe amplifier is designed to demonstrate the efficacy of the proposed technique.

II. Stability Theory

Many methods of assessing stability in multi-transistor circuits have been proposed in the literature [1]–[6]. For large multi-stage circuits, however, designers need a comprehensive workflow that can be utilized throughout the design process, and which has minimal simulation overhead.

Fig. 1(a) illustrates how a simple circuit with two transistors presents a complex stability picture with multiple internal loops and nodes that could potentially be unstable. K-factor would usually be employed to analyze the stability of this circuit. It is, however, a global two-port metric and valid only if the network is stable when ideally terminated [7]. Yet real-world circuits contain internal feedback paths that can introduce right half plane (RHP) poles that violate this assumption. Therefore, while K-factor may give some indication of instabilities, it should not be treated as a complete metric.

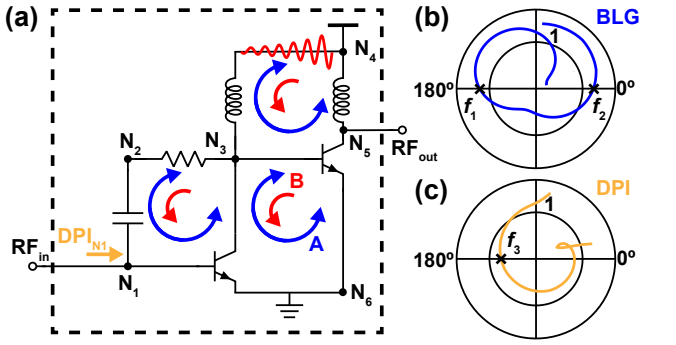

Fig. 1. (a) Example circuit showing nodal driving point immittance and three loops, with bilateral loops "A" and unilateral loops "B" illustrated, and which may not be captured by K-factor. (b) Bilateral loop gain plot showing two unstable frequencies, f_1 and f_2. (c) Driving point immittance plot showing one unstable frequency.

Mu-factor, unlike K-factor, which is a binary metric, can provide the proximity to oscillation across frequency. Unfortunately, since it is also a two-port global metric, internal feedback instabilities can easily be obscured.

Nyquist stability analysis identifies the frequencies at which a system will oscillate, by locating RHP poles. However, implementing this method requires sequentially breaking each feedback loop at the appropriate nodes. Additionally, unbreakable loops, such as those inherent within a device, can obscure the presence of these poles.

The NDF is computed from the Y-parameter matrix at all nodes in a circuit containing an active element that could cause a RHP pole. NDF is given by the ratio of the matrix determinant with the active devices enabled to the determinant with them disabled. Modern process design kits (PDKs) do not provide the designer access to internal active sources, so, in most cases, the NDF cannot be implemented as a rigorous stability solution.

Ohtomo's Network Bifurcation has similar implementation issues. In this method, the circuit is bifurcated into two networks, one containing the active elements and another

containing the passive elements. Circulators and isolators are applied to the active-passive interface nodes, and then a loop gain response is obtained for each that can be evaluated for oscillation conditions. For this technique to be valid, each network must be unconditionally stable. This isn't a reasonable assumption for modern high-gain, high-f_T devices, meaning that this function also cannot be easily implemented in a rigorous way.

A. Bilateral Loop Gain

Loop gain methods are another well-known technique to assess circuit instabilities caused by feedback [8]. Several methods have been used to accurately obtain the loop gain for a given node in a circuit. Classically, a test current was injected to measure the return ratio, but this can be inaccurate since it depends on the nodal impedance [9]. Middlebrook's null double injection technique [9] uses two auxiliary generators, a shunt current and series voltage source, to compensate for the impedance variation, and thus can be used at any point in the circuit. This method makes the assumption of unilateral signal flow, which fails to capture real feedback networks that have a bidirectional nature, as illustrated in Fig. 1(a).

Tian expanded Middlebrook's work for the bidirectional case with the true return ratio [10]. This allows for the bilateral loop gain to be calculated at any point in the circuit. Tian uses a similar method to Middlebrook but accounts for the reverse return ratio. The bilateral loop gain can be plotted on a polar plot and reviewed to check the local oscillation conditions. The magnitude of the loop gain must be greater than one and must cross the θ axis at either 0° or 180° in the clockwise direction, as shown in (1).

$$|LG| \geq 1 \quad \text{and} \quad \angle_{\text{cw}} LG \in \{0^\circ, 180^\circ\}. \tag{1}$$

where $\angle_{\text{cw}}$ denotes phase measured in the clockwise direction.

Loop gain methods are valuable when there are obvious loops in the circuit that need to be evaluated, but another metric is required at nodes where this is not the case.

B. Nodal Transfer Functions

When no clear loop can be identified, such as at device terminals, instabilities may still exist. These nodes must therefore be assessed via driving point immittance, the transfer function relating voltage to current at that node. To compute these values for a given node, auxiliary generators of voltage or current must be introduced that do not perturb the circuit. The authors in [11] propose voltage and current probes that do not draw any net power, and therefore do not disturb the operating point. These probes measure the current and voltage ratios at the node, and thus the driving point immittance for the node can be calculated.

The driving point impedance refers to the ratio of parallel voltage over parallel current, as shown in (2), and the driving point admittance is calculated from the series voltage and current, as shown in (3).

$$\text{DPI} = \frac{v_P}{i_P} \tag{2}$$

$$\text{DPA} = \frac{i_S}{v_S} \tag{3}$$

These transfer functions are used to inspect nodes of the circuit for oscillations. If there is an instability due to a series resonance, the driving point impedance will asymptote to infinity at the oscillation frequency. Conversely, if it is due to a parallel resonance, the driving point admittance will asymptote to infinity.

These functions are inverted and plotted on a polar chart, after which the Kurokawa conditions [12] are checked to determine the oscillation frequencies. The oscillation frequency is defined to be where the inverse of the function crosses the negative θ axis in a clockwise direction, as shown in (4).

$$\Re\left\{\tfrac{1}{DPI}\right\} \leq 0 \quad \text{and} \quad \angle_{\text{cw}}\left(\tfrac{1}{DPI}\right) = 180^\circ. \tag{4}$$

C. Design Implementation

The proposed approach leverages both the bilateral loop gain and driving point functions. These two complementary metrics can be used alongside traditional stability measures to give the designer greater insight into both loop- and nodal-level instabilities throughout the design process.

Designers can implement this approach with minimal overhead; for example, the Winslow Probe in Keysight ADS evaluates these metrics [13]. The probe is non-perturbative and provides direct outputs of the proposed metrics with only an S-parameter simulation. To provide a complete stability picture, the probe must be correctly placed in the circuit. Probes should be placed at all terminals of active devices (collector, base, emitter) as well as any other visible loops in the circuit (connected bias lines, ground loops, etc.).

Fig. 1(a) shows an example circuit, in order to help visualize which nodes need to be analyzed. The circuit has two active devices, as well as three visible loops. Nodes N_1, N_3, N_5, and N_6 at the device terminals and nodes N_2 and N_4 are in loops, so the loop gain and transfer functions should be evaluated at all of these nodes to look for oscillations.

After placing the probes, the bilateral loop gain, as well as the inverse of both driving point immittance functions, should be plotted in polar form and checked for the previously mentioned conditions. Fig. 1(b) illustrates an example with two unstable frequencies in the bilateral loop gain. Fig. 1(c) shows an example driving point immittance plot with one unstable frequency. The bilateral loop gain also quantifies proximity to oscillation since values of loop gain approaching unity signal a potential stability problem.

The advantage of this method is that once it is set up, the designer need only monitor the plots during the entire design process, similar to how K-factor is used. These metrics enable the designer to employ a proactive stability approach and fix issues as they arise during the entire design process.

III. Design Application

A. Circuit Stabilization

To demonstrate the proposed approach, a 20–40 GHz SiGe amplifier was designed in GlobalFoundries 90 nm SiGe BiC-

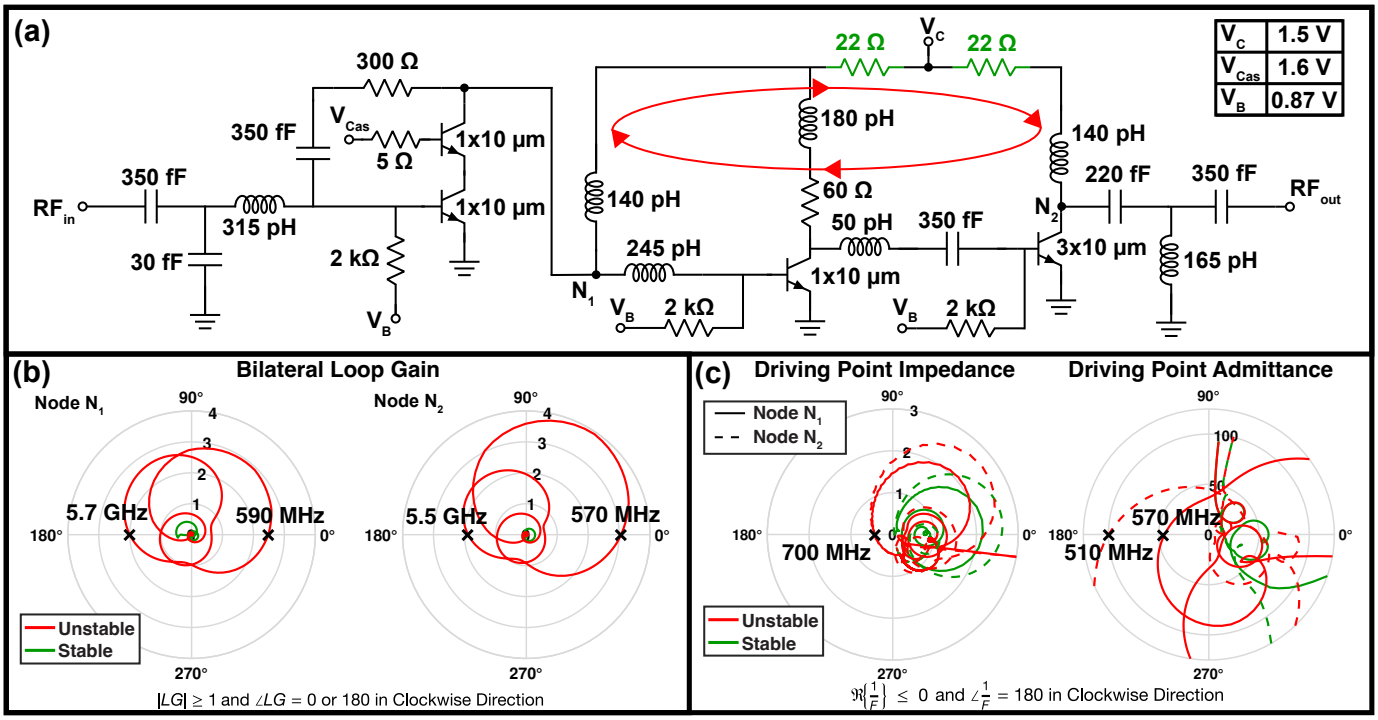

Fig. 2. (a) Amplifier schematic: feedback loop between first and third stages (red) and stabilization resistors (green). (b) Bilateral loop gain at nodes N_1 and N_2, with frequencies where oscillation conditions are met marked. (c) Driving point impedance and admittance at N_1 and N_2, with oscillation conditions and frequencies where they are met are marked.

MOS technology [14]. A schematic of the circuit is shown in Fig. 2(a). The first stage of the three-stage amplifier is a cascode topology, with resistive feedback used to increase the operating bandwidth. That stage is followed by two common-emitter (CE) stages. The last stage uses three parallel devices to increase output power.

The proposed stability approach was used during the design of this amplifier to ensure it was stable. The bilateral loop gain of all of the loops in the design and the driving point immittance of the active devices' nodes were analyzed throughout the design process to ensure that the oscillation conditions were not met.

During this design process, when the collectors of the three stages were connected, both the bilateral loop gain and the driving point immittance showed frequencies that met the oscillation condition.

For simplicity, the analysis will focus on nodes N_1 and N_2 in Fig. 2(a) even though other nodes, such as those in the loop, would show similar results. Within the collector loop, the bilateral loop gain shown in Fig. 2(b) shows the oscillation conditions being met at two frequencies, 590 MHz and 5.7 GHz, at node N_1 and, as expected, similar results at node N_2. The driving point immittance at nodes within the loop also show frequencies where the oscillation conditions are met. The driving point impedance shows an oscillation at 700 MHz when calculated at both nodes. At node N_1, the driving point admittance satisfies the conditions at 570 MHz, and node N_2 shows an oscillation at 510 MHz.

From these metrics, the circuit oscillates at approximately 500–700 MHz, and the problematic nodes and loops can be easily identified. This enables the designer to apply stabilization techniques only at the identified nodes, rather than adding resistors indiscriminately and degrading overall performance.

Series resistors, shown at the top of Fig. 2(a) in green, were added into the collector loop to stabilize the circuit. The green curves in bilateral loop gain and driving point immittance plots show the simulation results after adding the resistors. The functions no longer meet the oscillation condition, and thus the circuit is stable.

B. Measurement Results

Versions of the circuit with and without the stabilization resistors were fabricated and measured under the same bias conditions to demonstrate the effectiveness of the design method. The die micrograph is shown in Fig. 4. Measurements were performed with a Keysight N5227B PNA. A U8488A power sensor was used in the calibration for large-signal performance.

Since the oscillation was filtered before it reached the output, the frequency spectrum of the collector voltage (V_C) was measured directly. Fig. 3(c) displays this measurement for both versions, with the unstable version exhibiting the main oscillation tone at 624 MHz as well as its various high-frequency harmonics. This is within the frequency range obtained by the stability metrics. The stable version, however, as expected, shows a clean spectrum without any oscillation tones. The measured K-factor and Mu-factor are shown in

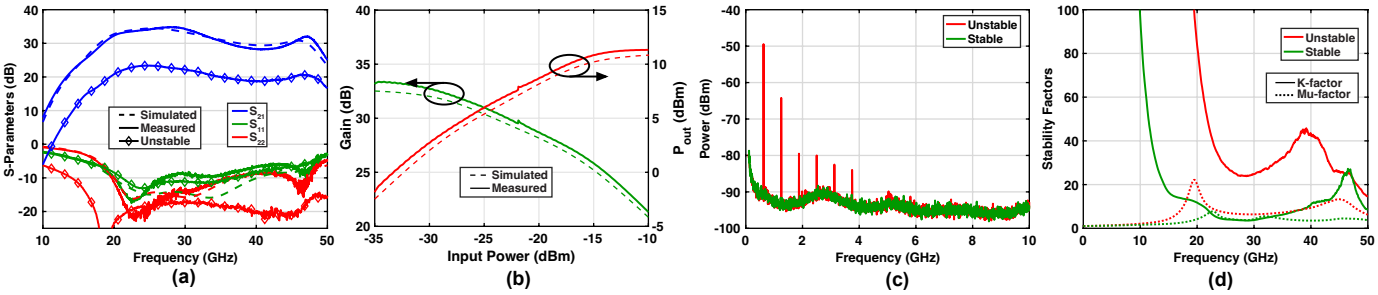

Fig. 3. Measurement and simulation results for the SiGe amplifiers. (a) S-Parameters for stable and unstable circuits. (b) Large-signal gain and output power versus input power for the stable circuit at 30 GHz. (c) Measured collector bias line frequency spectrum for stable and unstable versions. (d) Measured K-factor and Mu-factor for stable and unstable circuits, showing that the stability criteria are met.

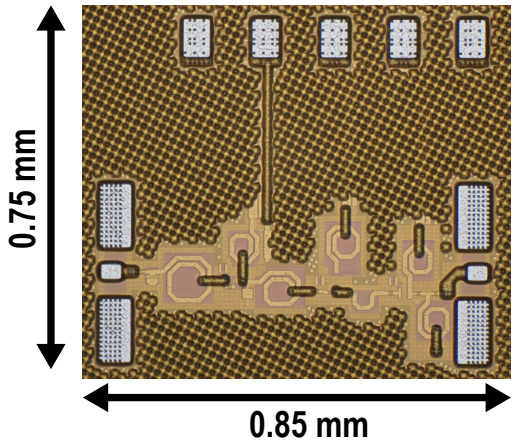

Fig. 4. Die micrograph of stable amplifier.

Fig. 3(d) and indicate that both versions meet the traditional criteria used for ensuring stability for these metrics. This was expected, as these metrics also indicated that the design was stable throughout the design process, and is likely due to the internal collector loop not being captured by these metrics.

The simulated and measured S-parameters for both versions are shown in Fig. 3(a). The measurement results of the stable amplifier show good agreement with simulations, while the unstable version shows an expected notable reduction in gain. Large-signal gain performance for the stable amplifier is shown in Fig. 3(b) and agrees well with simulations. The amplifier's measured power consumption is 42.5 mW and the OP_{1dB} is 5 dBm.

IV. Summary

This paper presented a new design approach for ensuring circuit stability using both nodal and loop analysis. The design-time approach presented empowers designers to comprehensively monitor stability throughout the design process. An application with a 20–40 GHz SiGe amplifier was demonstrated. The measurement results demonstrate that this technique not only stabilizes the circuit reliably, but also uncovers instabilities that conventional methods fail to identify. Moreover, the presented approach is broadly applicable across RF and mm-Wave designs, enabling designers to ensure stability with minimal added overhead.

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